REMARKS

Reconsideration of this application as amended is respectfully requested.

In the Office Action, claims 1-71 were pending and rejected. In this response, no claim has been canceled. Claims 1-3, 9, 24, 26-27, 40, 42-43, 56, and 58-59 have been amended. No new matter has been added.

The Examiner has rejected claims 1-13, 19-23 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,430,884 to Beard ("Beard"), in view of U.S. Patent No. 5,909,559 to So ("So"). Claims 14-18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Beard in view of So in view of U.S. Patent No. 6,597,745 to Dowling ("Dowling"). Claims 32, 48, 64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beard in view of So. Claims 34, 50, 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beard in view of Dowling. Claims 35, 36, 51, 52, 67, 68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beard in view of Dowling as applied to claim 34 above, and further in view of So. Claims 24-31, 33, 37-47, 49, 53-63, 65, 69-71 are rejected under 35 U.S.C. 102(b) as being anticipated by Beard.

In view of the foregoing amendments, it is respectfully submitted that claims 1-71 as amended include limitations that are not disclosed or suggested by the cited references. Specifically, for example, independent claim 1 requires a scalar processing unit and a vector processing unit implemented within a single chipset that interfaces one or more host processors and host memory with other components of a data processing system. For example, the single chipset may include a media processor having the scalar and vector processing units as a part of a north bridge of a data processing system. It is respectfully submitted that these limitations are absent from the cited references.

Although Beard discloses scalar/vector processors, such processors are part of multiple processors of a multi-processor machine. Thus, such processors are part of host processors and they are not implemented as part of chipset that interfaces (e.g., north bridge) the host processors and the rest of the components of a data processing system.

In addition, although So discloses a bus bridge device, So still fails to disclose chipset (e.g., a north bridge) interfacing the host processors and the rest of the components of the system having a scalar and vector processing units. Similarly, none of the other cited references discloses the limitations set forth above. Therefore, independent claim 1 is patentable over the cited references.

Similarly, independent claims 24, 40, and 56 include limitations similar to those discussed above. Thus, for the reasons similar to those discussed above, it is respectfully submitted that claims 24, 40, and 56 are patentable over the cited references.

Given that the rest of the claims depend from one of the above independent claims, for the reasons similar to those discussed above, it is respectfully submitted that the rest of the claims are patentable over the cited references. Withdrawal of the rejections is respectfully requested.

In view of the foregoing, Applicant respectfully submits the present application is now in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call the undersigned attorney at (408) 720-8300.

Please charge Deposit Account No. 02-2666 for any shortage of fees in connection with this response.

Respectfully submitted,

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Date: January 5, 2006

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